SEMESTER-I

SUBJECT CODES	SUBJECT NAME	**OFFERING DEPARTMENT	*COURSE NATURE (Hard/Soft/ Workshop/ NTCC)	COURSE TYPE (Core/Elective / University Compulsory)	L	T	P	O	NO. OF CONTACT HOURS PER WEEK	NO. OF CREDITS
ECH501B-T	RTL Simulation and Synthesis with PLDs	EC	HARD	CORE	3	0	0	0	3	3
ECH501B-P	RTL Simulation and Synthesis with PLDs Lab	EC	HARD	CORE	0	0	4	0	4	2
ECH502B-T	Microcontrollers and Programmable Digital Signal Processors	EC	HARD	CORE	3	0	0	0	3	3
ECH502B-P	Microcontrollers and Programmable Digital Signal Processors Lab	EC	HARD	CORE	0	0	4	0	4	2
ECH503B	Digital Signal and Image Processing	EC	HARD	ELECTIVE	3	0	0	0	3	3
ECH504B	Programming Languages for Embedded Software									
ECH505B	VLSI signal processing									
ECH506B	IOT and Applications									
ECH507B	Parallel Processing	EC	HARD	ELECTIVE	3	0	0	0	3	3
ECH508B	System Design with Embedded Linux									
ECH509B	CAD of Digital System									
ECS510B	Research Methodology and IPR	EC	SOFT	CORE	2	0	0	0	2	2
ECS511B	English for Research Paper Writing	EC	SOFT	AUDIT	2	0	0	0	0	0
	TOTAL (L-T-P-O/CONTACT HOURS/CREDITS)				**16**	**0**	**8**	**0**	**24**	**18**

Course Title/Code	**RTL Simulation and Synthesis with PLDs/ ECH501B-T/P**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-4-0
Course Objectives	To describe both simple and complex RTL design scenarios using VHDL. It gives practical information on the issues in ASIC prototyping using FPGAs, design challenges and how to overcome practical issues and concerns.

SECTION -A

Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.

SECTION -B

Design entry by Verilog/VHDL/FSM, Verilog AMS.

SECTION -C

Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection, Design for performance.

SECTION -D

Low power VLSI design techniques. Design for testability, IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping. Case studies and Speed issues.

Text/Reference Books

1.Richard S. Sandige, "Modern Digital Design", MGH, International Editions.
2.Donald D Givone, "Digital principles and Design", TMH
3.Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL", Cengage.

List of Experiments:

1. Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2. Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3. Vending machines - Traffic Light controller, ATM, elevator control.
4. PCI Bus & arbiter and downloading on FPGA.
5. UART/ USART implementation in Verilog.
6. Realization of single port SRAM in Verilog.
7. Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel adder/subtractor, serial/parallel multiplier.
8. Discrete Fourier transform/Fast Fourier Transform algorithm in Verilog.

Course Title/Code	**Microcontrollers and Programmable Digital Signal Processors/ ECH502B-T/P**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-4-0
Prerequisites	Microprocessor & interfacing
Course Objectives	Students will be able to 1. Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications. 2. Identify and characterize architecture of Programmable DSP Processors. 3. Develop small applications by utilizing the ARM processor core and DSP processor based platform.

SECTION A

ARM Cortex-M3 processor: Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

SECTION B

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency. LPC 17xx microcontroller-Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

SECTION C

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP-MAC unit, Barrel shifters, Introduction to TI DSP processor family

SECTION D

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations Code Composer Studio for application development for digital signal processing, On chip peripherals , Processor benchmarking.

References:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH , 2nd Edition
3. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication
4. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
5. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
6. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

List of Experiments:

Part A)

Experiments to be carried out on Cortex-M3 development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
    1. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
    2. UART Echo Test.
    3. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
    4. Temperature indication on an RGB LED.
    5. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.

6. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
7. System reset using watchdog timer in case something goes wrong.
8. Sample sound using a microphone and display sound levels on LEDs.

Part B)

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop an assembly code and C code to compute Euclidian distance between any two points
2. To develop assembly code and study the impact of parallel, serial and mixed execution
3. To develop assembly and C code for implementation of convolution operation
4. To design and implement filters in C to enhance the features of given input sequence/signal.

Course Title/Code	**Digital Signal and Image Processing/ ECH503B**
Course Type:	Elective (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	Calculus
Course Objectives	At the end of this course, students will be able to 1. Analyze discrete-time signals and systems in various domains 2. Design and implement filters using fixed point arithmetic targeted for embedded platforms 3. Compare algorithmic and computational complexities in processing and coding digital image.

SECTION A

Review of Discrete Time signals and systems, Characterization in time and Z and Fourier –domain, Fast Fourier Transform algorithms – In-place computations, Butterfly computations, bit reversal's.

SECTION B

Digital Filter design: FIR - Windowing and Frequency Sampling, IIR – Impulse invariance, bilinear Transformation. Fixed point implementation of filters – challenges and techniques.

SECTION C

Digital Image Acquisition, Enhancement, Restoration.Digital Image Coding and Compression – JPEG and JPEG 2000. Color Image processing – Handling multiple planes, computational challenges.

SECTION D

VLSI architectures for implementation of Image Processing algorithms, Pipelining.

References:

1. J.G. Proakis, Manolakis "Digital Signal Processing", Pearson, 4th Edition,Gonzalez and Woods, "Digital Image Processing", PHI, 3rd Edition
2. S. K. Mitra. "Digital Signal Processing – A Computer based Approach", TMH, 3rd Edition,2006
3. A. K. Jain, "Fundamentals of Digital Image Processing", Prentice Hall
4. KeshabParhi, "VLSI Digital Signal Processing Systems – Design and Implementation",Wiley India
5. Elective IProgramming Languages for Embedded Software

Course Title/Code	**Programming Languages for Embedded Software/ECH504B**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	C Language
Course Objectives	students will be able to 1. Write an embedded C application of moderate complexity. 2. Develop and analyze algorithms in C++. 3. Differentiate interpreted languages from compiled languages.

SECTION A

Embedded 'C' Programming -Bitwise operations, Dynamic memory allocation, OS services -Linked stack and queue, Sparse matrices, Binary tree -Interrupt handling in C, Code optimization issues -Writing LCD drives, LED drivers, Drivers for serial port communication -Embedded Software Development Cycle and Methods (Waterfall, Agile)

SECTION B

Object Oriented Programming -Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.
CPP Programming: 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.

SECTION C

Overloading and Inheritance: Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions.

SECTION D

Templates: Function template and class template, member function templates and template arguments,Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions.Scripting Languages Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

References:

1. Michael J. Pont , "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition 2011
3. A.Michael Berman, "Data structures via C++", Oxford University Press, 2002
4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey & Sons, 2005.

Course Title/Code	**VLSI Signal Processing/ ECH505B**
Course Type:	Elective (Departmental)

Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	Digital Signal processing
Course Objectives	At the end of this course, students will be able to 1.Acquire knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches. 2. Ability to acquire knowledge about retiming techniques, folding and register minimization.

SECTION A

Introduction to DSP systems, Pipelined and parallel processing, iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

SECTION B

Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise. Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

SECTION C

Numerical strength reduction, synchronous, wave and asynchronous pipe lines, low power design.

SECTION D

Programmable digital signal processors.

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References:

1. Keshab K. Parthi[A1] , VLSI Digital signal processing systems, design and
2. implementation[A2] , Wiley, Inter Science, 1999.
3. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing,
4. McGraw Hill, 1994
5. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall

Course Title/Code	**IOT and Applications /ECH506B**

Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	students will be able to 1. Understand the concept of IOT and M2M. 2. Study IOT architecture and applications in various fields.Study the security and privacy issues in IOT.

SECTION A

IoT& Web Technology The Internet of Things Today, Time for Convergence, Towards the IoT Universe, Internet of Things Vision, IoT Strategic Research and Innovation Directions, IoT Applications, Future Internet Technologies, Infrastructure, Networks and Communication, Processes, Data Management, Security, Privacy & Trust, Device Level Energy Issues, IoT Related Standardization, Recommendations on Research Topics.IoT Architecture -State of the Art – Introduction, State of the art, Architecture Reference Model-Introduction, Reference Model and architecture, IoT reference Model, IoT Reference Architecture- Introduction, Functional View, Information View, Deployment and Operational View, Other Relevant architectural views.

SECTION B

M2M to IoT – A Basic Perspective– Introduction, Some Definitions, M2M Value Chains, IoT Value Chains, An emerging industrial structure for IoT, The international driven global value chain and global information monopolies. M2M to IoT-An Architectural Overview– Building an architecture, Main design principles and needed capabilities, An IoT architecture outline, standards considerations.

SECTION C

IoT Applications for Value Creations Introduction, IoT applications for industry: Future Factory Concepts, Brownfield IoT, Smart Objects, Smart Applications, Four Aspects in your Business to Master IoT, Value Creation from Big Data and Serialization, IoT for Retailing Industry, IoT For Oil and Gas Industry, Opinions on IoT Application and Value for Industry, Home Management, eHealth.

SECTION D

Internet of Things Privacy, Security and Governance Introduction, Overview of Governance, Privacy and Security Issues, Contribution from FP7 Projects, Security, Privacy and Trust in IoT-Data-Platforms for Smart Cities, First Steps Towards a Secure Platform, Smartie Approach. Data Aggregation for the IoT in Smart Cities, Security

References:

1. Vijay Madisetti and ArshdeepBahga, "Internet of Things (A Hands-on-Approach)", 1st Edition, VPT, 2014.
2. Francis daCosta, "Rethinking the Internet of Things: A Scalable Approach to Connecting Everything", 1st Edition, Apress Publications, 2013.
3. CunoPfister, "Getting Started with the Internet of Things", OReilly Media, 2011.

Course Title/Code	**Parallel Processing/ ECH507B**
Course Type:	Elective (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	C language
Course Objectives	Student will be able to: 1. List various types of parallel computers and their architectures 2. Describe the concepts underlying the design, implementation, and use of message-passing computing and shared-memory computing.

Section A

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability. Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining.

Section B

VLIW processors Case study: Superscalar Architecture-Pentium, Intel Itanium Processor, Ultra SPARC, MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture.

Section C

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions, Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming,

Section D

Data Parallel Programming, Parallel Software Issues, Operating systems for multiprocessors systems, customizing applications on parallel processing platforms.

References:

1. Kai Hwang, Faye A. Briggs, "Computer Architecture and Parallel Processing", MGH International Edition
2. Kai Hwang, "Advanced Computer Architecture", TMH
3. V.Rajaraman, L. Sivaram Murthy, "Parallel Computers", PHI.
4. William Stallings, "Computer Organization and Architecture, Designing for performance" Prentice Hall, Sixth edition.
5. Kai Hwang, Zhiwei Xu, "Scalable Parallel Computing", MGH
6. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann.

Course Title/Code	**System Design with Embedded Linux/ ECH508B**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	students will be able to 1. Familiarity of the embedded Linux development model. 2. Write, debug, and profile applications and drivers in embedded Linux. 3. Understand and create Linux BSP for a hardware platform

SECTION A

Embedded Linux Vs Desktop Linux, Embedded Linux Distributions.Embedded Linux Architecture, Kernel Architecture – HAL, Memory manager, Scheduler, File System, I/O and Networking subsystem, IPC, User space, Start-up sequence.

SECTION B

Board Support Package Embedded Storage: MTD, Architecture, Drivers, Embedded File System Embedded Drivers: Serial, Ethernet, I2C, USB, Timer, Kernel Modules.

SECTION C

Porting Applications Real-Time Linux: Linux and Real time, Programming, Hard Real-time Linux.

SECTION D

Building and Debugging: Kernel, Root file system Embedded Graphics. Case study of uClinux.

References:

1. Karim Yaghmour, "Building Embededd Linux Systems", O'Reilly & Associates.
2. P Raghvan, Amol Lad, SriramNeelakandan, "Embedded Linux System Design and Development", Auerbach Publications Christopher Hallinan, "Embedded Linux Primer: A Practical Real World Approach", Prentice Hall, 2nd Edition, 2010.
3. Derek Molloy, "Exploring BeagleBone: Tools and Techniques for Building with Embedded Linux", Wiley, 1st Edition, 2014.

Course Title/Code	**CAD of Digital System/ ECH509B**
Course Type:	**Elective**
Course Nature:	SOFT
L-T-P-O Structure	3-0-0-0
Prerequisites	Digital System Design
Course Objectives	1.To understand the Fundamentals of CAD tools for modelling, design, test and verification of VLSI systems. 2. To Study of various phases of CAD, including simulation, physical design, test and verification. 3. To Demonstrate knowledge of computational algorithms and tools for CAD.·

SECTION A

Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, Fabrication Process and its impact on Design.

SECTION B

VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.

SECTION C

General purpose methods for combinational optimization – partitioning, floor planning and pin assignment, placement , routing.

SECTION D

Simulation – logic synthesis, verification, high level Synthesis, MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

References:

1. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation".
2. S.H. Gerez, "Algorithms for VLSI Design Automation.

Course Title/Code	**Research Methodology and IPR/ECS510B**
Course Type:	Core (Departmental)
Course Nature:	Soft
L-T-P-O Structure	3-0-0-0
Course Objectives	students will be able to 1. Understand research problem formulation. 2. Analyze research related information 3. Follow research ethics 4. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

	5. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular. 6. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

SECTION A

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

SECTION B

Effective literature studies approaches, analysis Plagiarism, Research ethics. Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

SECTION C

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

SECTION D

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

References:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"
3. Ranjit Kumar, 2nd Edition , "Research Methodology: A Step by Step Guide for beginners" Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
4. Mayall , "Industrial Design", McGraw Hill, 1992.
5. Niebel , "Product Design", McGraw Hill, 1974.

6. Asimov , “Introduction to Design”, Prentice Hall, 1962.
7. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “ Intellectual Property in New Technological Age”, 2016.
8. T. Ramappa, “Intellectual Property Rights Under WTO”, S. Chand, 2008

Course Title/Code	**English for Research Paper Writing /ECS511B**
Course Type:	Core (Departmental)
Course Nature:	Soft
L-T-P-O Structure	2-0-0-0
Course Objectives	students will be able to 1. Understand that how to improve your writing skills and level of readability 2. Learn about what to write in each section 3. Understand the skills needed when writing a Title Ensure the good quality of paper at very first-time submission

SECTION A

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness, Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts. Introduction.

SECTION B

Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check.

SECTION C

key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature

SECTION D

skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions, useful phrases, how to ensure paper is as good as it could possibly be the first-time submission.

References:

1 Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books)
2 Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3 Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book .
4 Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

SEMESTER-II

SUBJECT CODES	SUBJECT NAME	**OFFERING DEPARTMENT	*COURSE NATURE (Hard/Soft/ Workshop/ NTCC)	COURSE TYPE (Core/Elective/ University Compulsory)	L	T	P	O	NO. OF CONTACT HOURS PER WEEK	NO. OF CREDITS
ECH512B-T	Analog and Digital CMOS VLSI Design	EC	HARD	CORE	3	0	0	0	3	3
ECH512B-P	Analog and Digital CMOS VLSI Design Lab	EC	HARD	CORE	0	0	4	0	4	2
ECH513B-T	VLSI Design Verification and Testing	EC	HARD	CORE	3	0	0	0	3	3
ECH513B-P	VLSI Design Verification and Testing Lab	EC	HARD	CORE	0	0	4	0	4	2
ECH514B	Memory Technologies	EC	HARD	ELECTIVE	3	0	0	0	3	3
ECH515B	Communication Buses and Interfaces									
ECH516B	Low power VLSI Design									
ECH517B	SoC Design	EC	HARD	ELECTIVE	3	0	0	0	3	3
ECH518B	Network Security and Cryptography									
ECH519B	Physical design automation									
ECN520B	Mini Project	EC	NTCC	CORE	0	0	4	0	4	2
ECS521B	Pedagogy Studies	EC	SOFT	AUDIT	2	0	0	0	0	0
	TOTAL (L-T-P-O/CONTACT HOURS/CREDITS)				**14**	**0**	**12**	**0**	**26**	**18**

Course Title/Code	**Analog and Digital CMOS VLSI Design/ECH512B-T/P**
Course Type:	Core
Course Nature:	Hard
L-T-P-O Structure	3-0-4-0
Prerequisites	Analog Integrated Circuits & Digital Electronics
Course Objectives	students will be able to 1. Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics. 2. Connect the individual gates to form the building blocks of a system. 3. Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Section A

Digital CMOS Design:

Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption.

Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model.Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

Section B

Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

Section C

Analog CMOS Design:

Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

Section D

Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

References:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi , "Design of Analog CMOS Integrated Circuits", TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3rd Edition.
5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

List of Experiments:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.

d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV To extract Vth use the following procedure. i. Plot gm vs VGS using NGSPICE and obtain peak gm point. ii. Plot y=ID/(gm)1/2 as a function of VGS using Ngspice. iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate your result according to technologies and comment on it.
2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
a) Perform the following
i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.
ii. Plot VTC for CMOS inverter with varying VDD.
iii. Plot VTC for CMOS inverter with varying device ratio.
b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf. (use VPULSE = 2V, Cload = 50fF)
c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use Cin= 0.012pF, Cload = 4pF, Rload = k)
3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and time period.
4) Perform the following
a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13um process.
b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L)MN=5, (W/L)MP=10 and L=0.5um for both transistors.
i. Establish a test bench, as explained in the lecture, to achieve VDSQ=VDD/2.
ii. Calculate input bias voltage if bias current=50uA.
iii.Use Ngspice and obtain the bias current. Compare its value with 50uA.
iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
v.Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW.
vi. Use Ngspice to determine input voltage range of the amplifier .
5) Three OPAMP INA. Vdd=1.8V Vss=0V, CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
i. Draw the schematic of op-amp macro model.

ii. Draw the schematic of INA.
iii. Obtain parameters of the op-amp macro model such that
a. low-frequency voltage gain = 5x104,
b. unity gain BW (fu) = 500KHz,
c. input capacitance=0.2pF,
d. output resistance =�,
e. CMRR=120dB
iv. Draw schematic diagram of CMRR simulation setup.
v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
vi.Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.
6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Microwind.
a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
c) Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
d) Use interconnect length obtained and connect the second and third inverter. Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part 'c'.

Course Title/Code	**VLSI Design Verification and Testing/ECH513B-T/P**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-4-0
Prerequisites	VlSI DESIGN
Course Objectives	1.To get familiar with Front end design and verification techniques and create reusable test environments. 2. To Verify increasingly complex designs more efficiently and effectively. 3. To use EDA tools like Cadence, Mentor Graphics.

SECTION-A

Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.

SECTION-B

Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef , Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

SECTION-C

Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions,

SECTION-D

SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

References:

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design,Specification, and Verification Language).
4. System Verilog website – www.systemverilog.org
5. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilogEvents.pdf
6. General reuse information and resources www.design-reuse.com

7. OVM, UVM(on top of SV) www.verificationacademy.com
8. Verification IP resources
   http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
   http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/defa ult.aspx

List of Experimnts:

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions

Course Title/Code	**Memory Technologies/ ECH514B**
Course Type:	Core
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	Students will be able to: • Select architecture and design semiconductor memory circuits and subsystems. • Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures. • Knowhow of the state-of-the-art memory chip design

SECTION-A

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.

SECTION-B

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

SECTION-C

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

SECTION-D

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

References:

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
2. Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
3. Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

Course Title/Code	**Communication Buses and Interfaces ECH515B**
Course Type:	Elective
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	
Course Objectives	students will be able to: • Select a particular serial bus suitable for a particular application. • Develop APIs for configuration, reading and writing data onto serial bus. • Design and develop peripherals that can be interfaced to desired serial bus.

SECTION A

Serial Busses -Physical interface, Data and Control signals, features.Limitations and applications of RS232, RS485, I2C, SPI

SECTION B

CAN -Architecture, Data transmission, Layers, Frame formats, applications**,** PCIe -Revisions, Configuration space, Hardware protocols, applications

SECTION C

USB -Transfer types, enumeration, Descriptor types and contents, Device driver

SECTION D

Data Streaming Serial Communication Protocol -Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

References:

1. Jan Axelson, "Serial Port Complete -COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems ", Lakeview Research, 2nd Edition
2. Jan Axelson, "USB Complete", Penram Publications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", Mindshare Press
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition, 2005.
5. Serial Front Panel Draft Standard VITA 17.1 – 200x
6. Technical references on www.can-cia.org, www.pcisig.com, www.usb.org

Course Title/Code	**Low Power VLSI Design/ECH516B**
Course Type:	Elective
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	VLSI Design
Course Objectives	Students will be able to 1. Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability. 2. Characterize and model power consumption & understand the basic analysis methods. 3. Understand leakage sources and reduction techniques.

Section A

Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of Vdd & Vt on speed, constraints on Vt reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations.

Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches.

Section B

Low Power Clock Distribution: Power dissipation in clock distribution, single driver versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. tolerable skew, chip & package co-design of clock network.

Section C

Logic Synthesis for Low Power estimation techniques: Power minimization techniques, low power arithmetic components-circuit design styles, adders, multipliers.

Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits,low power SRAM circuits.

Section D

Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance.

References:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995•
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998**.**

Course Title/Code	**SOC Design/ECH517B**
Course Type:	Elective (Departmental)
Course Nature:	Hard

L-T-P-O Structure	3-0-0-0
Prerequisites	Digital System Design
Course Objectives	Student will be able to 1. Understand What SoC is and what the differences between SoC and Embedded System System. 2. Design Methodology in SoC Design Flow and Design Tools.

Section A

ASIC -Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts. NISC -NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP)

Section B

No-Instruction-Set-computer (NISC)-design flow, modeling NISC architectures and systems, use of Generic Netlist Representation -A formal language for specification, compilation and synthesis of embedded processors. Simulation -Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

Section C

Low power SoC design / Digital system, -Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification. Synthesis -Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph.

Section D

Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis. Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs. Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization. *Note:* Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of theory course.

References:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008.

2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3. RochitRajsuman, "System-on-a-chip: Design and test", Advantest America R & D Center, 2000
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

Course Title/Code	**Network Security and Cryptography /ECH518B**
Course Type:	Elective
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	students will be able to: • Select a particular serial bus suitable for a particular application. • Develop APIs for configuration, reading and writing data onto serial bus. • Design and develop peripherals that can be interfaced to desired serial bus.

SECTION-A

Security -Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques. Number Theory -Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

SECTION-B

Private-Key (Symmetric) Cryptography -Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis. Public-Key (Asymmetric) Cryptography -RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

SECTION-C

Authentication -IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction.

SECTION-D

System Security -Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems.

References:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
3. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
4. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Title/Code	**Physical Design Automation/ECH519B**
Course Type:	Elective (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	RTL Simulation and Synthesis with PLDs

Course Objectives	1. Understand the concepts of Physical Design Process such as partitioning,Floorplanning, Placement and routing. 2. Discuss the concepts of design optimization algorithms and their application to physical design automation. 3. Understand the concepts of simulation and synthesis in VLSI Design Automation. 4. Formulate CAD design problems using algorithmic methods.

Section A

Introduction to VLSI Physical Design Automation, Standard cell, Performance issues in circuit layout, delay models Layout styles.

Section B

Discrete methods in global placement, Timing-driven placement, Global Routing Via Minimization.

Section C

Over the Cell Routing -Single layer and two-layer routing, Clock and Power Routing.

Section D

Compaction, algorithms, Physical Design Automation of FPGAs..

References:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2nd Edition
3. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
4. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2nd Edition
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

Course Title/Code	**Pedagogy Studies/ ECS521B**
Course Type:	Audit
Course Nature:	Soft
L-T-P-O Structure	3-0-0-0
Course Objectives	Students will be able to: 1. Review existing evidence on the review topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers. 2. Identify critical evidence gaps to guide the development.

Section A

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.
Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

Section B

Evidence on the effectiveness of pedagogical practices, Methodology for the in depth stage: quality assessment of included studies.
How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

Section C

Professional development: alignment with classroom practices and follow-up support, Peer Support from the head teacher and the community.
Curriculum and assessment, Barriers to learning: limited resources and large class sizes.

Section D

Research gaps and future directions
Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

References:

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261.
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379.
3. Akyeampong K (2003) Teacher training in Ghana -does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID.
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
5. Alexander RJ (2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
6. Chavan M (2003) Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

SEMESTER-III

SUBJECT CODES	SUBJECT NAME	**OFFERING DEPARTMENT	*COURSE NATURE (Hard/Soft/ Workshop/ NTCC)	COURSE TYPE (Core/Elective/ University Compulsory)	L	T	P	O	NO. OF CONTACT HOURS PER WEEK	NO. OF CREDITS
ECH601B	Communication Network	EC	HARD	ELECTIVE	3	0	0	**0**	**3**	3
	Selected Topics in Mathematics									
ECH602B	Nano materials and Nanotechnology									
ECH603B	RF and Microwave Circuit Design									
	Operations Research		HARD	ELECTIVE	3	0	0	0	3	3
	Cost Management of Engineering Projects									
	Waste to Energy									
ECN605B	Dissertation Phase – I	EC	NTCC	CORE	0	0	20	0	20	10
	TOTAL (L-T-P-O/CONTACT HOURS/CREDITS)				**6**	**0**	**20**	**0**	**26**	**16**

Course Title/Code	**Communication Network/ECH601B**
Course Type:	Elective (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	At the end of the course, students will demonstrate the ability to: 1. Understand advanced concepts in Communication Networking 2. Design and develop protocols for Communication Networks. 3. Understand the mechanisms in Quality of Service in networking 4. Optimize the Network Design.

SECTION-A

Overview of Internet-Concepts, challenges and history. Overview of -ATM. TCP/IP Congestion and Flow Control in Internet-Throughput analysis of TCP congestion control. TCP for high bandwidth delay networks. Fairness issues in TCP. Real Time Communications over Internet. Adaptive applications. Latency and throughput issues.

SECTION-B

Integrated Services Model (intServ). Resource reservation in Internet. RSVP;Characterization of Traffic by Linearly Bounded Arrival Processes (LBAP). Leaky bucket algorithm and its properties. Packet Scheduling Algorithms-requirements and choices. Scheduling guaranteed service connections. GPS, WFQ and Rate proportional algorithms.

SECTION-C

High speed scheduler design. Theory of Latency Rate servers and delay bounds in packet switched networks for LBAP traffic; Active Queue Management - RED, WRED and Virtual clock. Control theoretic analysis of active queue management. IP address lookup-challenges. Packet classification algorithms and Flow Identification-Grid of Tries, Cross producing and controlled prefix expansion algorithms.

SECTION-D

Admission control in Internet. Concept of Effective bandwidth. Measurement based admission control. Differentiated Services in Internet (DiffServ). DiffServ architecture and framework.
IPV4, IPV6, IP tunneling, IP switching and MPLS, Overview of IP over ATM and its evolution to IP switching. MPLS architecture and framework. MPLS Protocols. Traffic engineering issues in MPLS.

References:

1. Jean Wairand and PravinVaraiya, "High Performance Communications Networks", 2nd edition, 2000.
2. Jean Le Boudec and Patrick Thiran, "Network Calculus A Theory of Deterministic Queueing Systems for the Internet", Springer Veriag, 2001.
3. Zhang Wang, "Internet QoS", Morgan Kaufman, 2001.
4. Anurag Kumar, D. Manjunath and Joy Kuri, "Communication Networking: An Analytical Approach" , Morgan Kaufman Publishers, 2004.
5. George Kesidis, "ATM Network Performance", Kluwer Academic, Research Papers, 2005.

Course Title/Code	**Selected Topics in Mathematics**
Course Type:	Core
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	Students will be able to : 1. Characterize and represent data collected from experiments using statistical methods. 2. Model physical process/systems with multiple variables towards parameter estimation and prediction 3. Represent systems/architectures using graphs and trees towards optimizing desired objective.

SECTION A

Probability and Statistics: -Definitions, conditional probability, Bayes Theorem and independence. -Random Variables: Discrete, continuous and mixed random variables, probability mass, probability density and cumulative distribution functions, mathematical expectation, moments, moment generating function, Chebyshev inequality.

SECTION B

Special Distributions: Discrete uniform, Binomial, Geometric, Poisson, Exponential, Gamma, Normal distributions. -Pseudo random sequence generation with given distribution, Functions of a Random Variable

SECTION C

Joint Distributions: Joint, marginal and conditional distributions, product moments, correlation, independence of random variables, bi-variate normal distribution. -Stochastic Processes: Definition and classification of stochastic processes, Poisson process -Norms, Statistical methods for ranking data
Multivariate Data Analysis -Linear and non-linear models, Regression, Prediction and Estimation -Design of Experiments – factorial method -Response surface method

SECTION D

Graphs and Trees: -Graphs: Basic terminology, multi graphs and weighted graphs, paths and circuits, shortest path Problems, Euler and Hamiltonian paths and circuits, factors of a graph, planar graph and Kuratowski's graph and theorem, independent sets, graph colouring
Trees: Rooted trees, path length in rooted trees, binary search trees, spanning trees and cut set, theorems on spanning trees, cut sets , circuits, minimal spanning trees, Kruskal's and Prim's algorithms for minimal spanning tree

References:

1. Henry Stark, John W. Woods, "Probability and Random Process with Applications to Signal Processing", Pearson Education, 3rd Edition
2. C. L. Liu, "Elements of Discrete Mathematics", Tata McGraw-Hill, 2nd Edition
3. Douglas C. Montgomery, E.A. Peck and G. G. Vining, "Introduction to Linear Regression Analysis", John Wiley and Sons, 2001.
4. Douglas C. Montgomery, "Design and Analysis of Experiments", John Wiley and Sons, 2001.
5. B. A. Ogunnaike, "Random Phenomena: Fundamentals of Probability and Statistics for Engineers", CRC Press, 2010.

Course Title/Code	**Nanomaterials and Nanotechnology/ECH602B**
Course Type:	Elective (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Course Objectives	To provide students with the basic concept and scientific foundation to enter the world of nanomaterials and nanotechnology.

Section A

Nanomaterials in one and higher dimensions, Applications of one and higher dimension nano-materials.

Section B

Nano-lithography, micro electro-mechanical system (MEMS) and nano-phonics.

Section C

Carbon nanotubes – synthesis and applications

Section D

Interdisciplinary arena of nanotechnology

References:

1. Nanoscale Materials in Chemistry edited by Kenneth J. Klabunde and Ryan M. Richards, 2ndedn, John Wiley and Sons, 2009.
2. Nanocrystalline Materials by A I Gusev and A ARempel, Cambridge International Science Publishing, 1st Indian edition by Viva Books Pvt. Ltd. 2008.
3. Springer Handbook of Nanotechnology by Bharat Bhushan, Springer, 3rdedn, 2010.
4. Carbon Nanotubes: Synthesis, Characterization and Applications by Kamal K. Kar, Research Publishing Services; 1stedn, 2011, ISBN-13: 978-9810863975..

Course Title/Code	**RF and Microwave Circuit Design/ ECH603B**
Course Type:	Core (Departmental)
Course Nature:	Hard
L-T-P-O Structure	3-0-0-0
Prerequisites	Basic Knowledge of Electromagnetic Fields & Waves and Microwave Engineering
Course Objectives	Design, analysis, optimization and characterization of miniaturized RF and microwave circuits using new breakthroughs in microwave theory and techniques.

Section A

Transmission Line Theory:Lumped element circuit model for transmission line, field analysis, Smith chart, quarter wave transformer, generator and load mismatch, impedance matching and tuning. Microwave Network Analysis: Impedance and equivalent voltage and current, Impedance and admittance matrix, The scattering matrix, transmission matrix, Signal flow graph.

Section B

Microwave Components: Microwave resonators, Microwave filters, power dividers and directional couplers, Ferromagnetic devices and components. Nonlinearity And Time Variance Inter-symbol interference, random process & noise, definition of sensitivity and dynamic range, conversion gain and distortion.

Section C

Microwave Semiconductor Devices And Modeling: PIN diode, Tunnel diodes, Varactor diode, Schottky diode, IMPATT and TRAPATT devices, transferred electron devices, Microwave BJTs, GaAs FETs, low noise and power GaAs FETs, MESFET, MOSFET, HEMT.

Section D

Amplifiers Design: Power gain equations, stability, impedance matching, constant gain and noise figure circles, small signal, low noise, high power and broadband amplifier, oscillators, Mixers design.

References:

1. Matthew M. Radmanesh, "Advanced RF & Microwave Circuit Design: The Ultimate Guide to Superior Design", AuthorHouse, 2009.
2. D.M.Pozar, " Microwave engineering" ,Wiley, 4th edition, 2011.
3. R.Ludwig and P.Bretchko, "R. F. Circuit Design", Pearson Education Inc, 2009.
4. G.D. Vendelin, A.M. Pavoi, U. L. Rohde, "Microwave Circuit Design Using Linear And Non Linear Techniques", John Wiley 1990.
5. S.Y. Liao, "Microwave circuit Analysis and Amplifier Design", Prentice Hall 1987.
6. Radmanesh, "RF and Microwave Electronics Illustrated" , Pearson Education, 2004.

SEMESTER-IV

SUBJECT CODES	SUBJECT NAME	**OFFERING DEPARTMENT	*COURSE NATURE (Hard/Soft/ Workshop/ NTCC)	COURSE TYPE (Core/Elective/ University Compulsory)	L	T	P	O	NO. OF CONTACT HOURS PER WEEK	NO. OF CREDITS
ECN605B	Dissertation Phase – II	EC	NTCC	CORE	0	0	32	0	32	16
	TOTAL (L-T-P-O/CONTACT HOURS/CREDITS)				**0**	**0**	**32**	**0**	**32**	**16**

Course Title/Code	Dissertation Phase – II/ECN606B
Course Type:	Core (Departmental)
Course Nature:	NTCC
L-T-P-O Structure	0-0-32-0
Course Objectives	At the end of this course, students will be able to 1. Ability to synthesize knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem. 2. Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design. 3. Ability to present the findings of their technical solution in a written report. 4. Presenting the work in International/ National conference or reputed journals

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study. The dissertation should have the following

i. Relevance to social needs of society
ii. Relevance to value addition to existing facilities in the institute
iii. Relevance to industry need
iv. Problems of national importance
v. Research and development in various domain The student should complete the following:

vi. Literature survey Problem Definition
vii. Motivation for study and Objectives
viii. Preliminary design / feasibility / modular approaches
ix. Implementation and Verification
x. Report and presentation The dissertation stage II is based on a report prepared by the students on dissertation allotted to them. It may be based on:
    a. Experimental verification / Proof of concept.
    b. Design, fabrication, testing of Communication System.
    c. The viva-voce examination will be based on the above report and work.

Guidelines for Dissertation Phase – I and II at M. Tech. (Electronics):

As per the AICTE directives, the dissertation is a year long activity, to be carried out and evaluated in two phases i.e. Phase – I: July to December and Phase – II: January to June.
The dissertation may be carried out preferably in-house i.e. departments laboratories and centers OR in industry allotted through departments T & P coordinator.

1. After multiple interactions with guide and based on comprehensive literature survey, the student shall identify the domain and define dissertation objectives. The referred literature should preferably include IEEE/IET/IETE/Springer/Science Direct/ACM journals in the areas of Computing and Processing (Hardware and Software), Circuits-Devices and Systems, Communication-Networking and Security, Robotics and Control Systems, Signal Processing and Analysis and any other related domain. In case of Industry sponsored projects, the relevant application notes, while papers, product catalogues should be referred and reported.
2. Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and phase wise work distribution, and submit the proposal within a month from the date of registration.

a. Phase – I deliverables: A document report comprising of summary of literature survey, detailed objectives, project specifications, paper and/or computer aided design, proof of concept/functionality, part results, A record of continuous progress.
b. Phase – I evaluation: A committee comprising of guides of respective specialization shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend repeating the Phase-I work.
c. During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences OR IP/Patents. P
d. hase – II deliverables: A dissertation report as per the specified format, developed system in the form of hardware and/or software, A record of continuous progress.
e. Phase – II evaluation: Guide along with appointed external examiner shall assess the progress/performance of the student based on report, presentation and Q & A. In case of unsatisfactory performance, committee may recommend for extension or repeating the work.