MANAV RACHNA
vidyanatariksha

MANAV RACHNA UNIVERSITY
(FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING
NAAC ACCREDITED 'A' GRADE INSTITUTION)
Declared as State Private University under section 2f of the UGC act, 1956

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

"T3-Examination, May-2018"

Semester:6th
Subject:Digital System Design
Branch: CST
Course Type: Core
Time: 3 Hours
Max.Marks: 80

Date of Exam:18/05/2018
Subject Code:ECH318-T
Session: I
Course Nature: Hard
Program: B.Tech
Signature: HOD/Associate HOD:

PART-A

All questions are compulsory.

Q1(a). Define combinational circuits and sequential circuits. (10*2=20)
(b). Why VHDL simulation is required?
(c). Write VHDL syntax of entity declaration.
(d). Write application of state diagrams.
(e). Write truth-table of S-R flip-flops & T flip-flops.
(f). Differentiate between Moore FSM & Mealy FSM.
(g). Why choose a CPLD over a FPGA.
(h). Differentiate between PLA & PAL PLD's.
(i). Define GAL.
(j). Define PEEL.

PART-B

Attempt any two questions.

Q2(a). Write VHDL code for 4:1 Multiplexer in behavioral model using case statement. (7)
(b). Write VHDL code for 4 bit digital comparator for behavioral model. (8)
Q3(a). Write VHDL code for 3 bit UP-DOWN Asynchronous Counter. (10)
(b). How to decide whether to use Moore FSM & Mealy FSM? Explain. (5)
Q4(a). Explain the Moore machine and Mealy machine with their diagrams and explain them. (8)
(b). Write VHDL code for PISO shift registers. (7)

PART-C

Attempt any two questions.

Q5(a). Realize Full Adder equations of Sum & Carry using PLA. (10)
(b). Draw & explain the structure of ROM with suitable example. (5)
Q6(a). What is PAL? Draw & explain its structure with example. (5)
(b). Write VHDL code for ALU. (10)
Q7. Attempt the following & explain with diagram (15)
(a). FPGA
(b). CPLD
(c). GAL

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