MANAV RACHNA vidyanatariksha

MANAV RACHNA UNIVERSITY
(FORMERLY MANAV RACHNA COLLEGE OF ENGINEERING
NAAC ACCREDITED 'A' GRADE INSTITUTION)
Declared as State Private University under section 2f of the UGC act, 1956

DEPARTMENT OF CST

"T3 Examination, May- 2018"

Semester:IV
Subject: COMPUTER ARCHITECTURE & ORGANISATION
Branch:CSE
Course Type: CORE
Time: 3 Hours
Max.Marks: 80

Date of Exam:15/05/2018
Subject Code: CSH210-T
Session: Morning
Course Nature: HARD
Program: B.Tech
Signature: HOD/Associate HOD:

Note: All questions are compulsory from Part-A(2*10=20 Marks).Attempt any two Questions from Part-B(Each Question carry 15 Marks). Attempt any two Questions from Part-C(Each Question carry 15 Marks).

PART-A (Each Question carries 2 Marks)

Q.1 a) Which one is the fastest memory in computer and why.
b) Design RAM chip for 8085 microprocessor.
c) What are the Hit and Miss ratio in Cache memory.
d) Differentiate between write through and write back policies in cache memory.
e) Why is mapping required and also state all types of mapping.
f) Design control unit for multiple micro-operations.
g) Explain the Locality of reference principle.
h) Explain the Amdahl's Law of performance.
i) Explain working of sequencer in microprogrammed control organization.
j) Differentiate between instruction format and microinstruction format.

PART-B (ATTEMPT ANY TWO QUESTIONS) (Each Question carries 15 Marks)

Q.2 a) i)How many 128 x 8 RAM chips are needed to provide a memory capacity of 2048 bytes?
ii) How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips? [6]
b) What are the different types of interrupts? Explain how an I/O interrupt can be handled with the help of interrupt cycle. [9]
Q.3 a) State different modes of transfer. Explain working of DMA controller with the help of block diagram. [9]
b) A digital computer has a memory unit of 64K x 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.
i) How many bits are there in the tag, index, block, and word fields of the address format?
ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit. [6]

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Q.4 a) Design and explain the concept of expanded memory with the help of four RAMs (128 * 8 words) and a ROM (512 * 8 words). [9]

b) The access time of a cache memory is 100ns and that of main memory 1000ns. It is estimate that 80% of the memory requests are for read and the remaining 20% for write. The hit ratio for read accesses only is 0.9. A write-through procedure is used.

i)What is the average access time of the system considering only memory read cyles?

ii)What is the average access time of the system for both read and write requests? [6]

PART-C (ATTEMPT ANY TWO QUESTIONS)(Each Question carries 15 Marks)

Q.5 a) Design and explain the Microprogram Sequencer. [6]

b) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. [9]

Q.6 a) What is pipelining. Differentiate between synchronous and asynchronous pipelining. [6]

b) In certain scientific computations it is necessary to perform the arithmetic operation (Ai+Bi)(Ci+Di) with a stream of numbers. Specifiy a pipeline configuration to carry out this task. List the contents of all registers in the pipeline for i=1 through 6. [9]

Q.7 a) Explain the microinstruction format for the control memory in detail with the help of flow chart. [8]

b) What are the drawbacks in pipelining? Explain various dependency problems in pipelining.[7]

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